



U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

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**INFORMATION DISCLOSURE STATEMENT  
UNDER 37 CFR 1.97**

(Use several sheets if necessary)

APPLICANTS  
Robert Allen Castlebary et al.

FILING DATE  
October 23, 2003

GROUP  
2631

**U.S. PATENT DOCUMENTS**

EXAMINE INITIAL		DOCUMENT NUMBER	ISSUE DATE	APPLICANT/PATENTEE	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE
LW	AA	5,761,254	6/2/1998	Behrin	375	355	

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	PUBL. DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION Yes No	

**OTHER INFORMATION (Including Author, Title, Pub.Date, Pertinent Pages, Country, Etc.)**

LW	AB		Park J-Y et al.: "A 1.0 GBPS CMOS Oversampling Data Recovery Circuit with Fine Delay Generation Method" IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Institute of Electronics Information and Comm. Eng. Tokyo, JP, Vol. E83-A, No. 6 13 July 1999 (1999-07-13), Pages 1100-1105, XP001032162					

EXAMINER /Lawrence Williams/ (11/30/2006) DATE CONSIDERED

SUBMITTED BY:

Robert B. Levy

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